Abstract of the Disclosure

An apparatus and method for regenerating reset and clock signals and a high-speed digital system using the apparatus and method are provided. In the regenerating circuit of the invention, a clock circuit receives an external clock signal and generates therefrom an internal clock signal, which is forwarded to a plurality of clocked circuits such as, for example, D flip-flops. A reset circuit receives an external reset signal and generates therefrom an internal reset signal, which is forwarded to the clocked circuits to reset the clock circuits. A clock masking circuit masks the internal clock signal for a masking period such that the clocked circuits are not clocked during the masking period. The high-speed digital system of the invention includes a plurality of function blocks coupled on a bus. The reset and clock regenerating circuit of the invention generates internal reset and clock signals from externally applied reset and clock signals.

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